Semiconductor Manufacturing Using EUV Lithography

Progress and Remaining Challenges

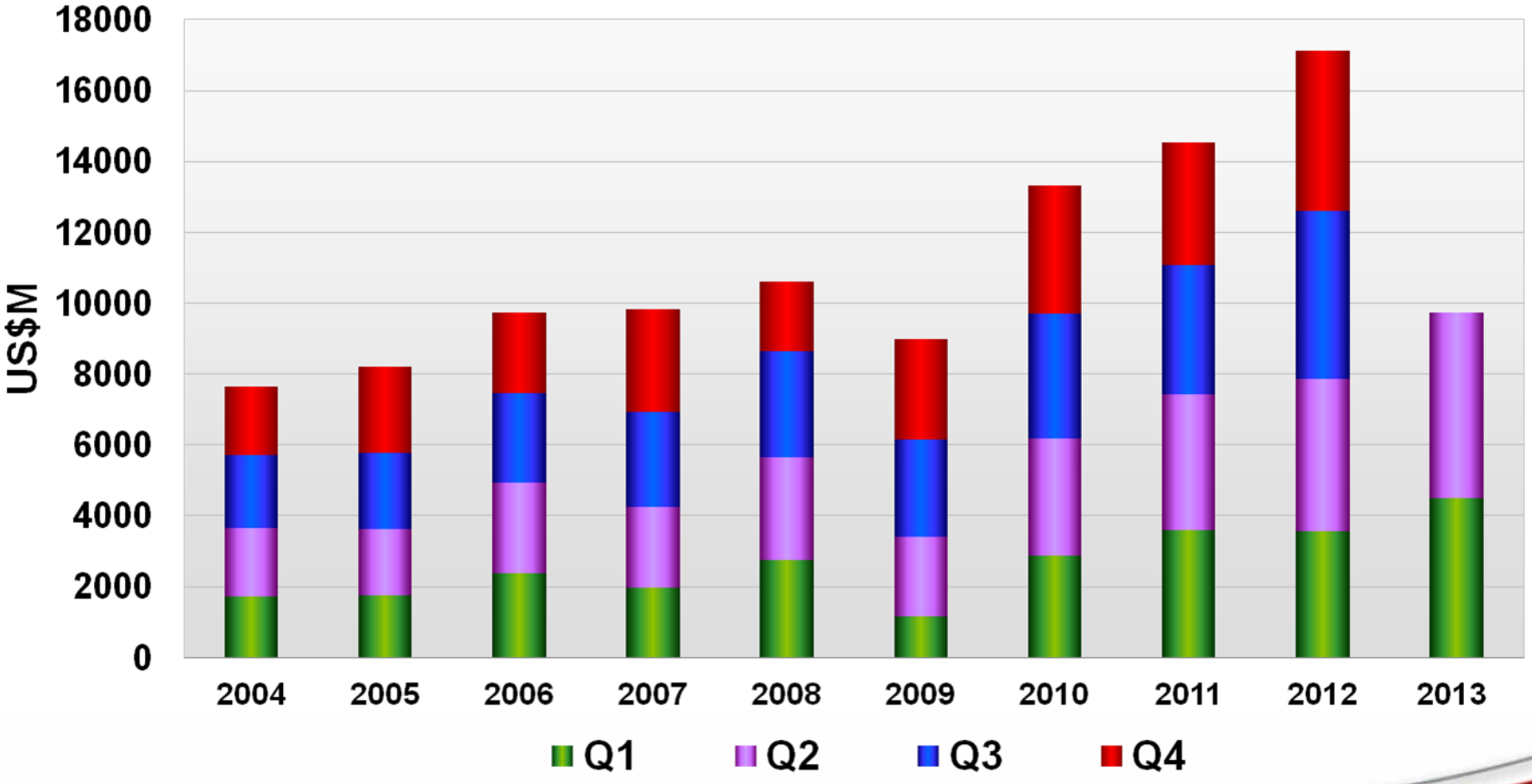
Anthony Yen

7 October 2013

TSMC Property

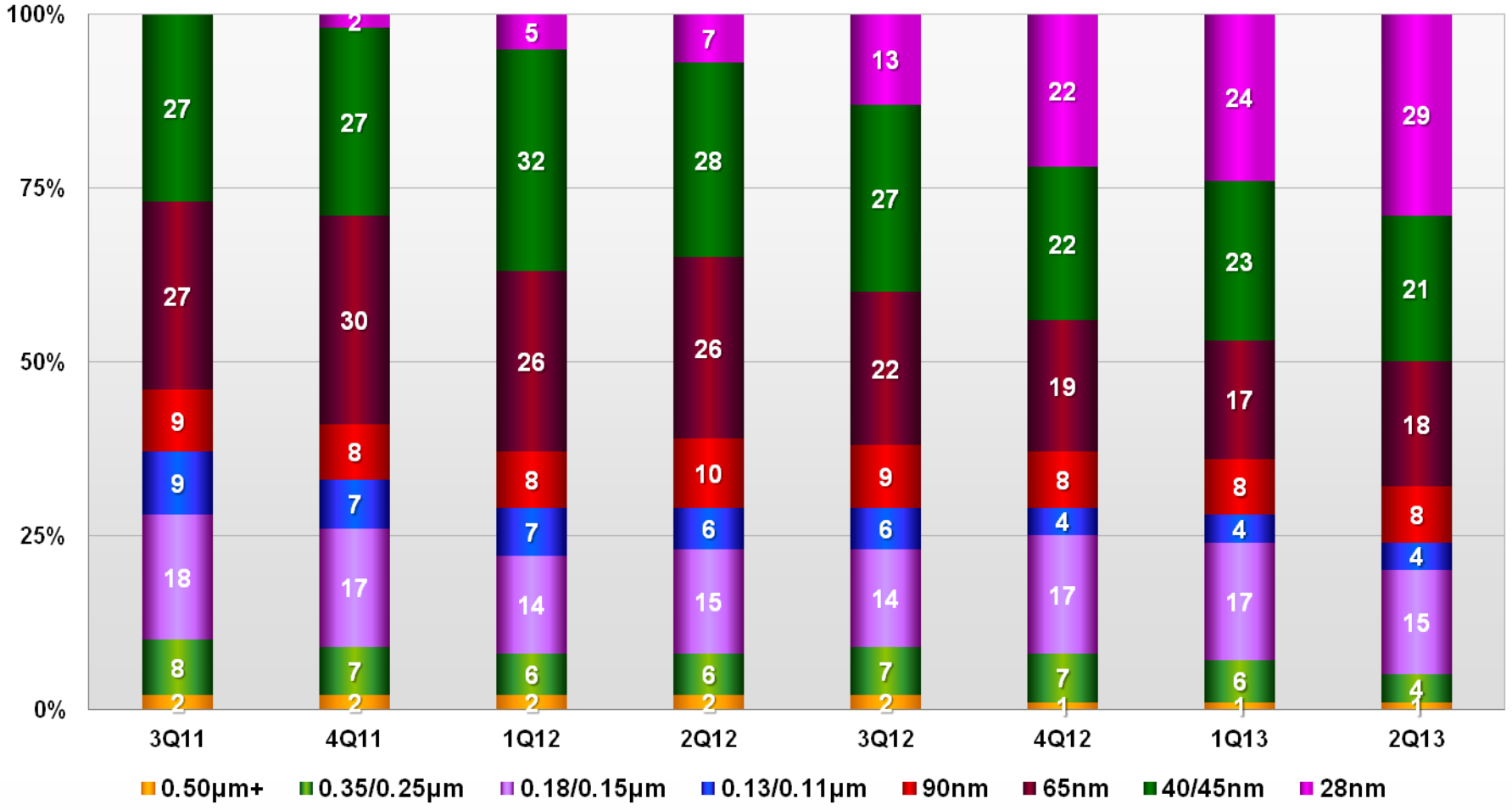
TSMC Sales Growth

2Q 2013 Sales US$5.23B



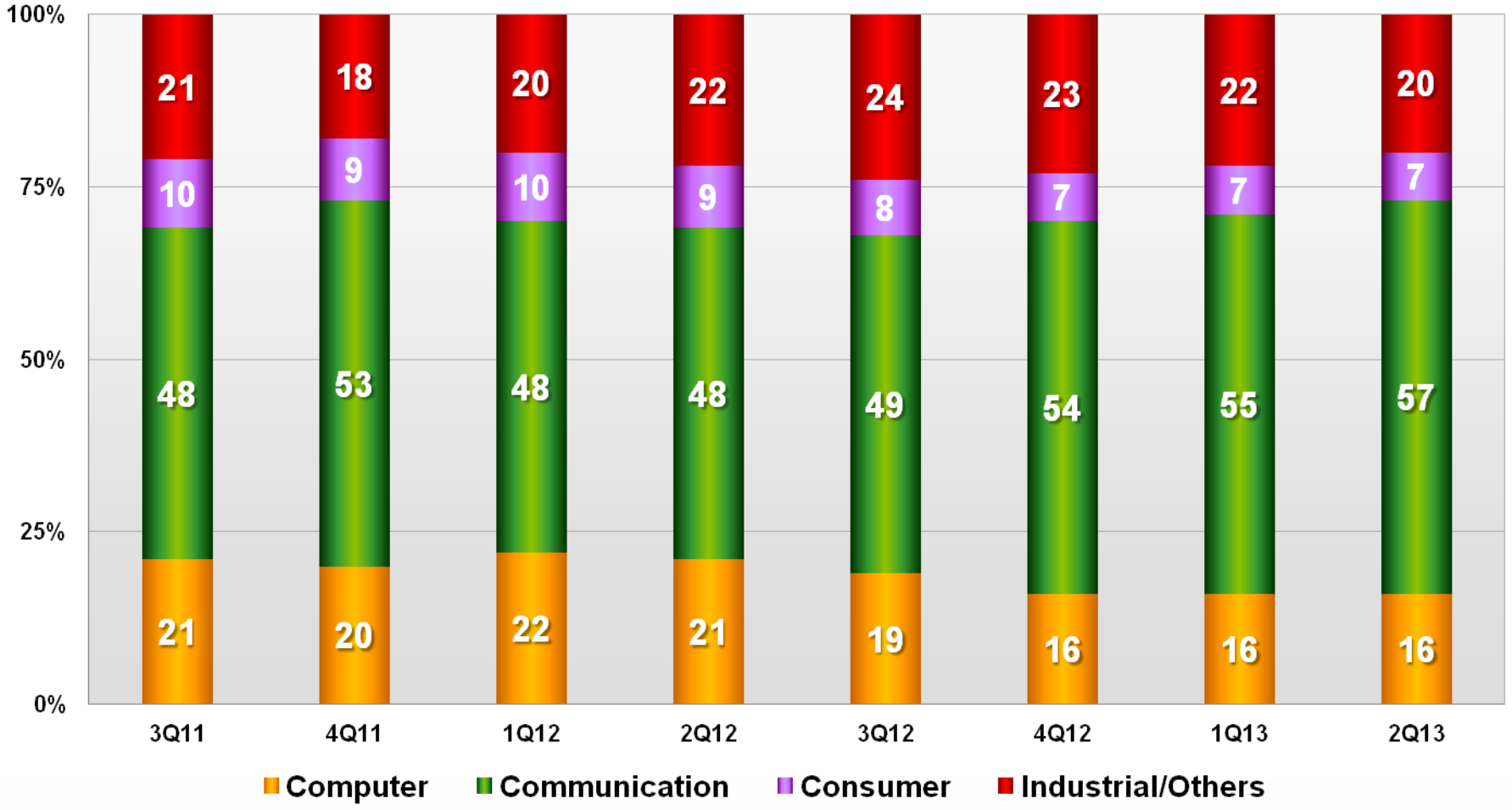
TSMC Property

Sales Breakdown by Technology

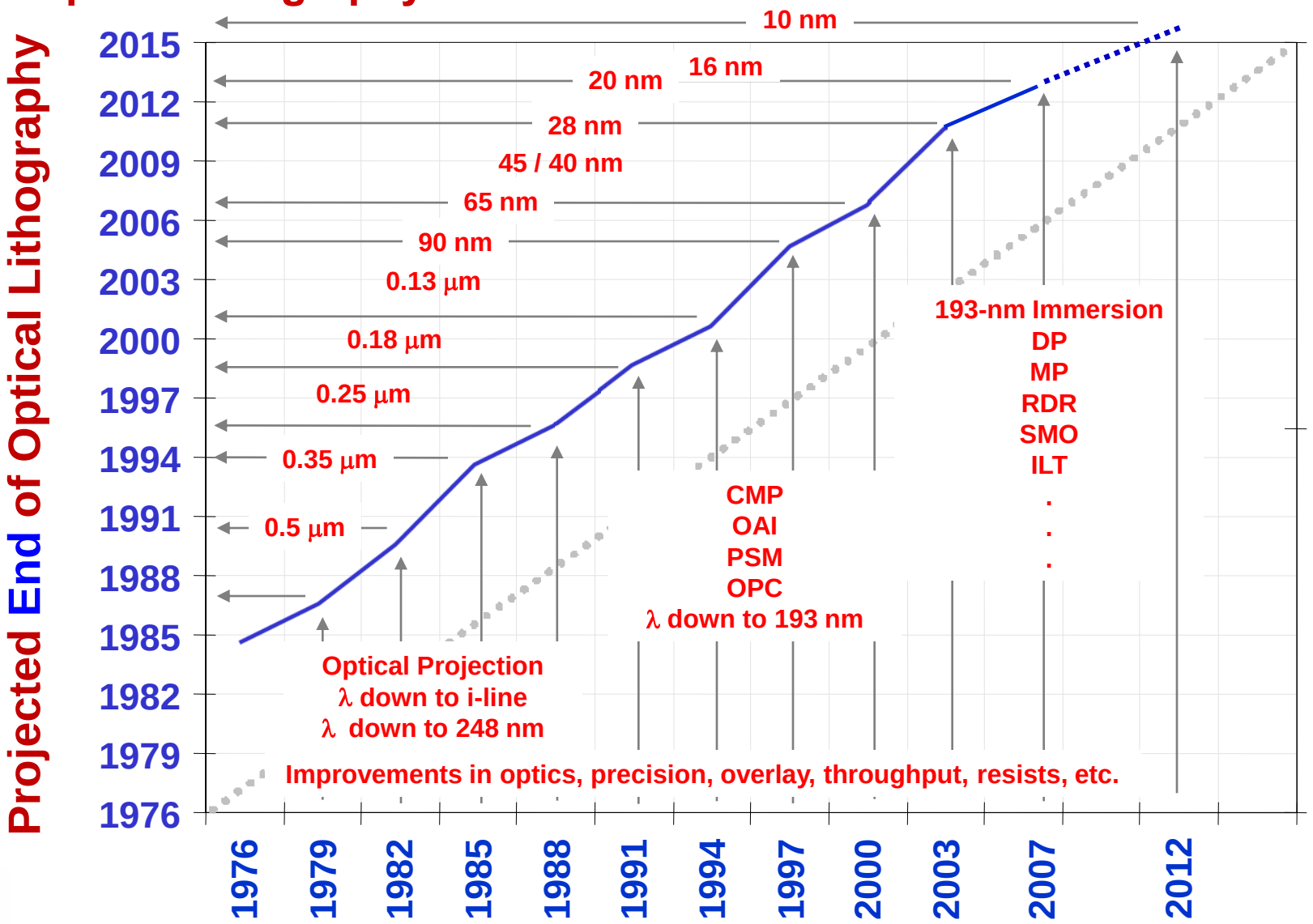


TSMC Property

Sales Breakdown by Application

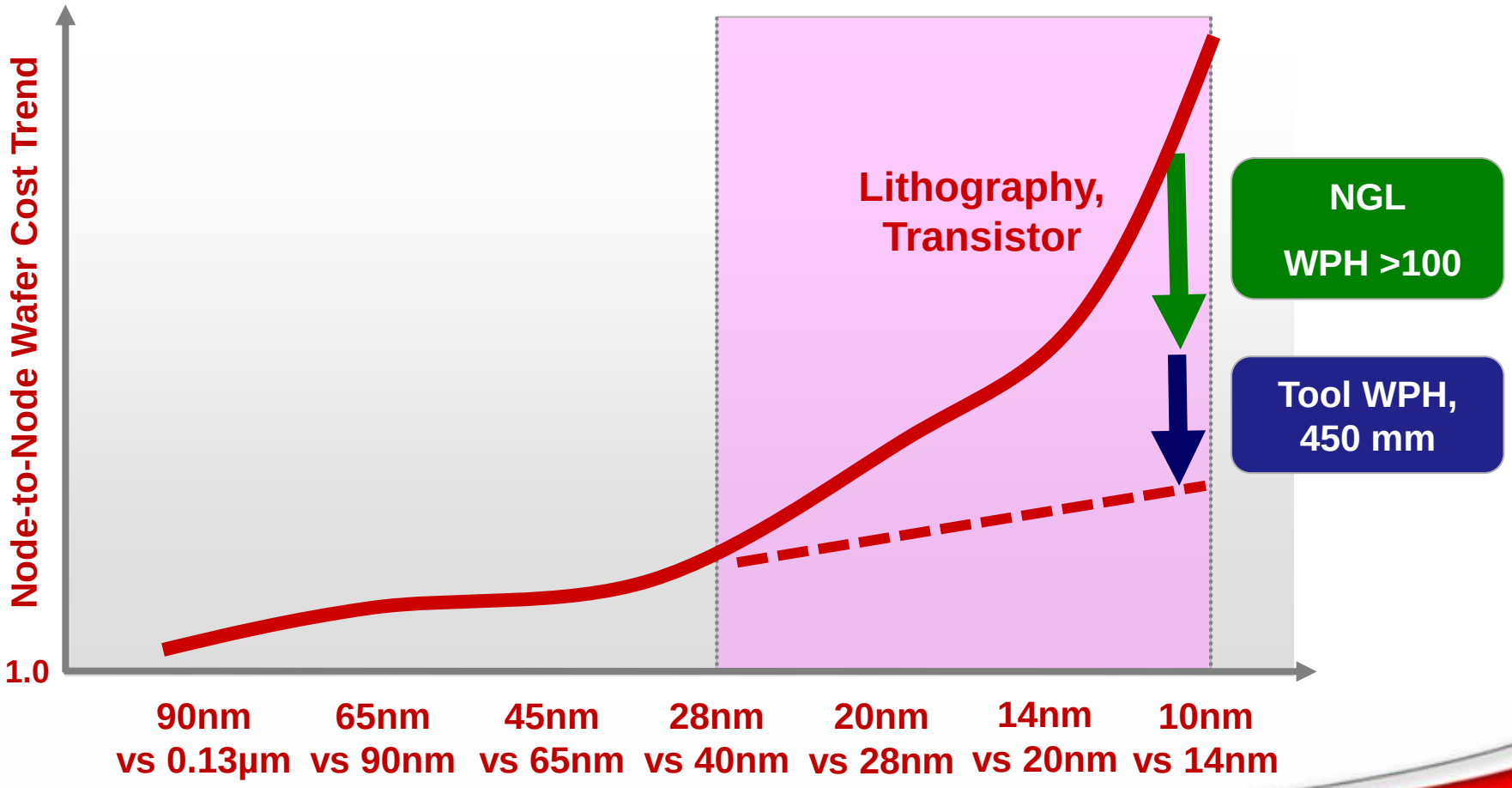


Optical lithography has sustained Moore's law for ~ 5 decades

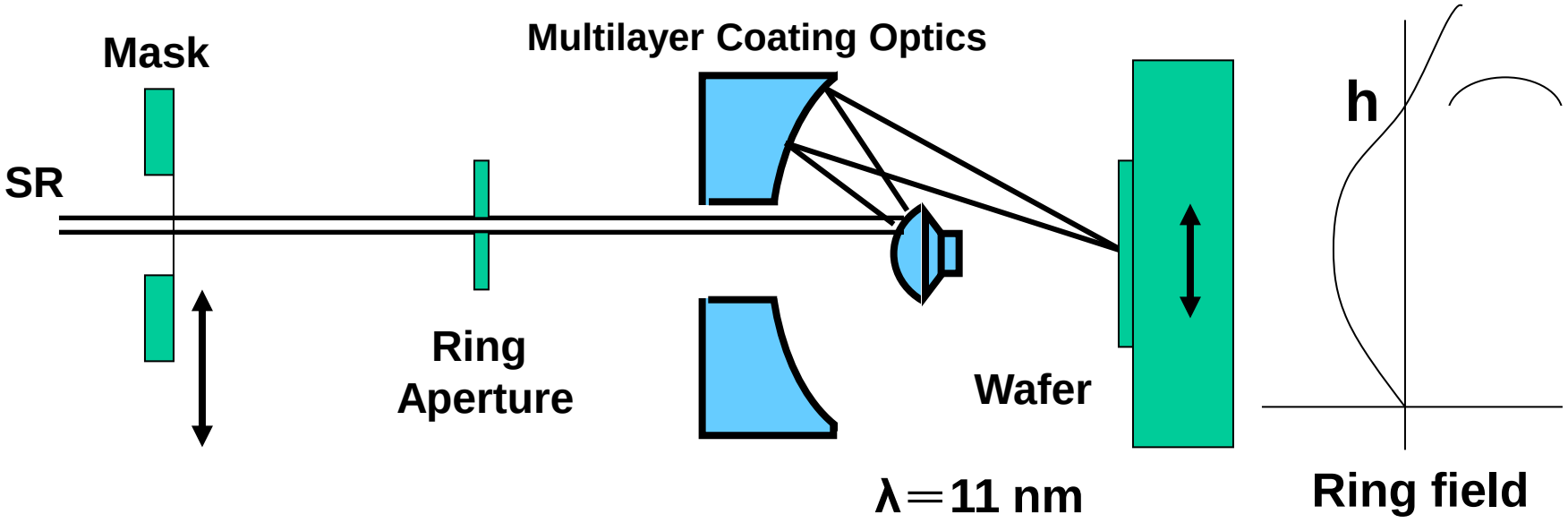


J. Sturtevant, B.J. Lin, A. Yen

Node-to-Node Wafer Cost Trend



NTT Experiments on EUV Lithography



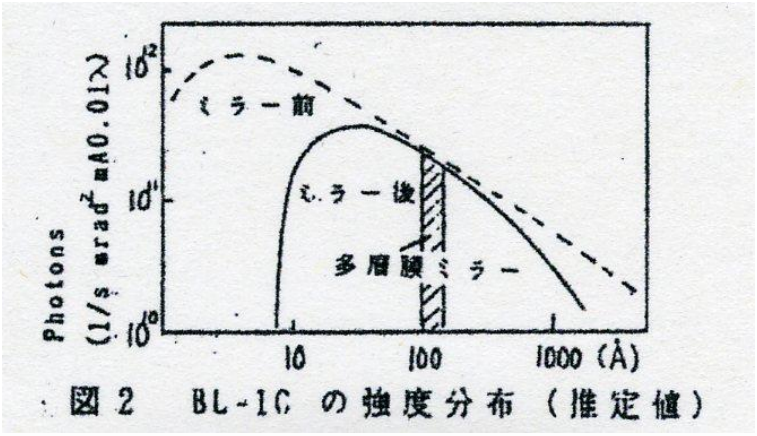


図 2　BL-1C の強度分布（推定値）

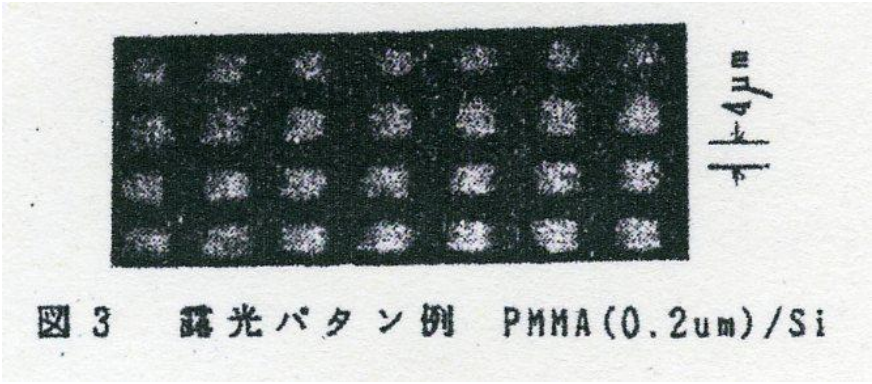
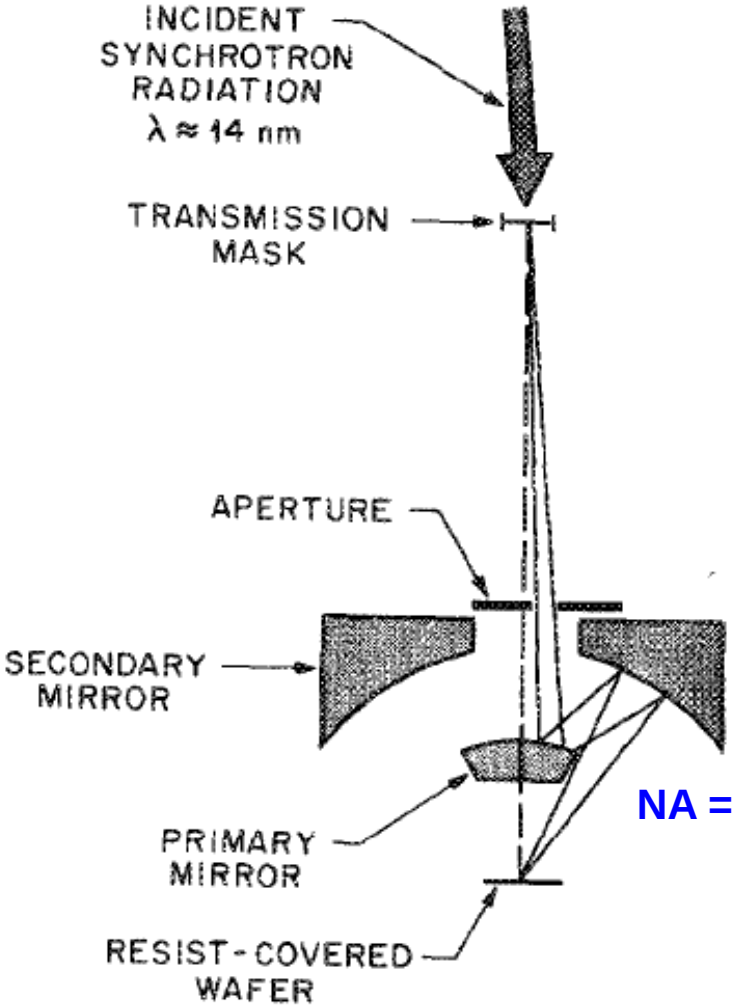


図 3　露光パタン例　PMMA(0.2um)/Si

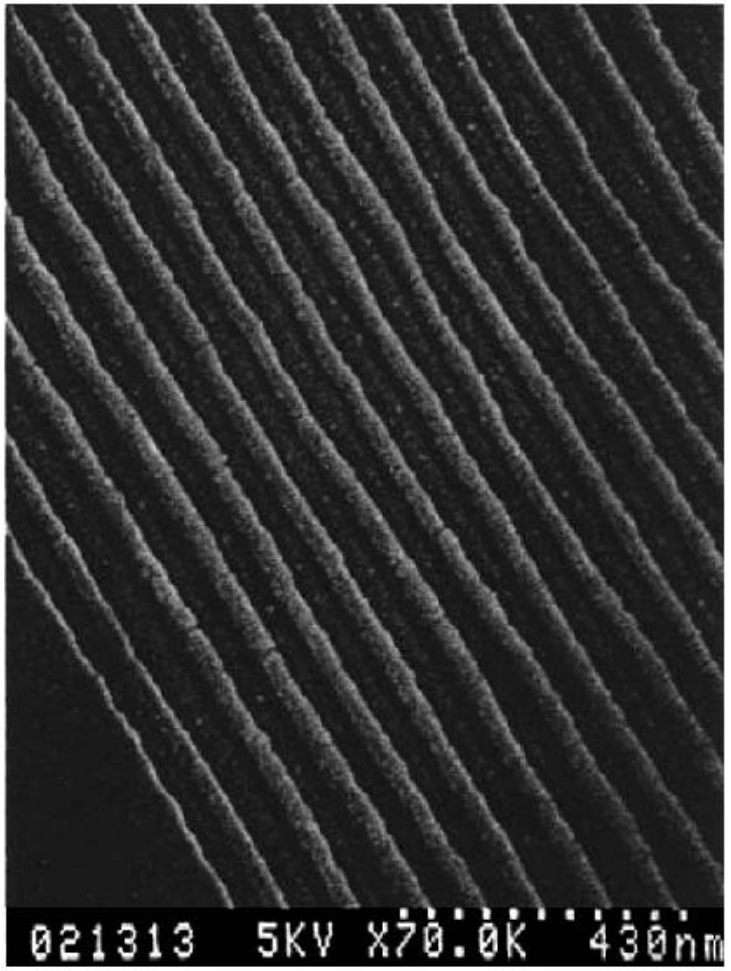
Kinoshita et al., the 47th Autumn Meeting, Japan Society of Applied Physics, 1986

Slide Courtesy of Hiroo Kinoshita

Bell Lab Experiments on EUV Lithography



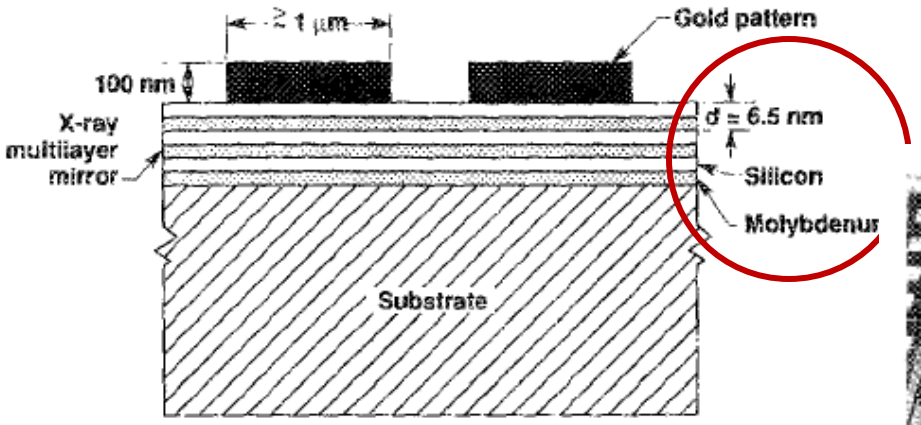
NA = 0.08

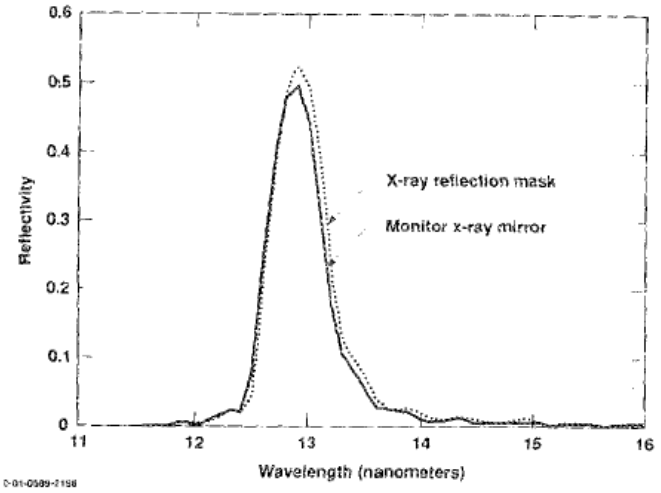


Pitch = 100 nm

Bjorkholm et al., JVST B 8, 1509, Nov/Dec 1990

Reflective EUV Mask Proposed and Fabricated





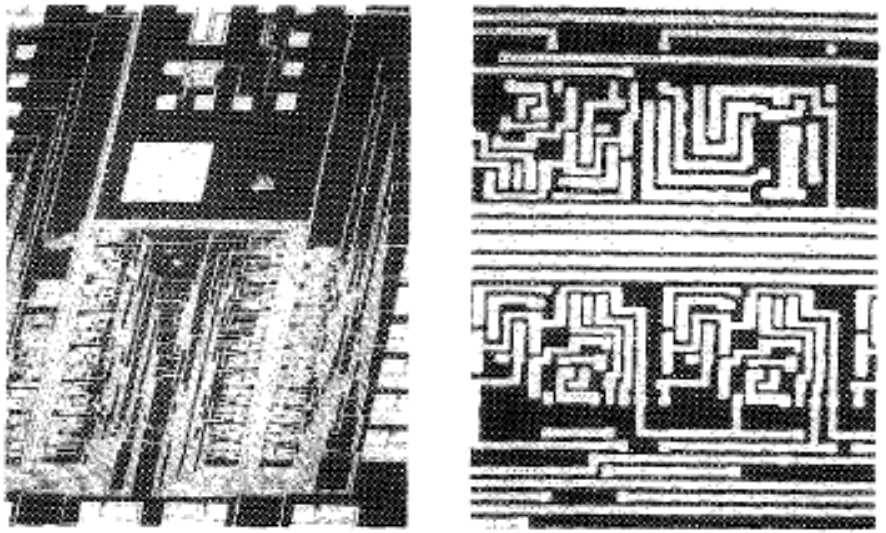


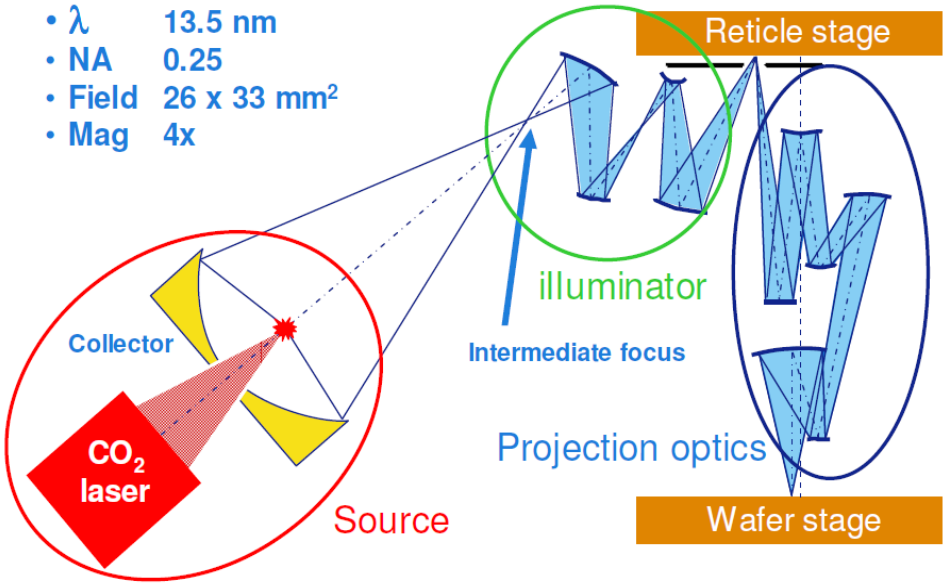
FIG. 3. Scanning electron micrographs of an XRPL mask. The bright regions are areas of 100 nm thick gold, patterned onto a soft x-ray multilayer mirror.

Hawryluk et al., JVST B7, 1702, Nov/Dec 1989

EUV Lithography Using NXE3100

NXE3100 EUV scanner exposing wafers at TSMC since Nov 2011

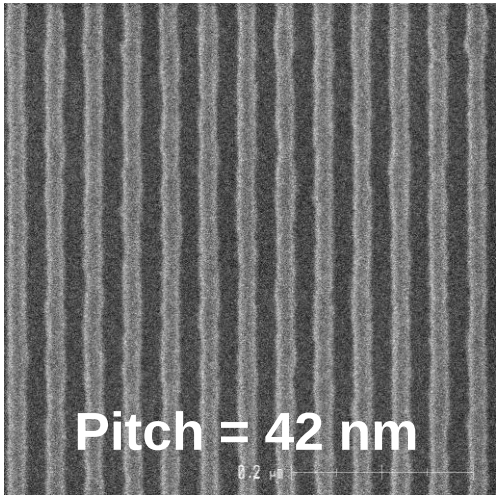
- λ 13.5 nm
- NA 0.25
- Field 26 x 33 mm²
- Mag 4x

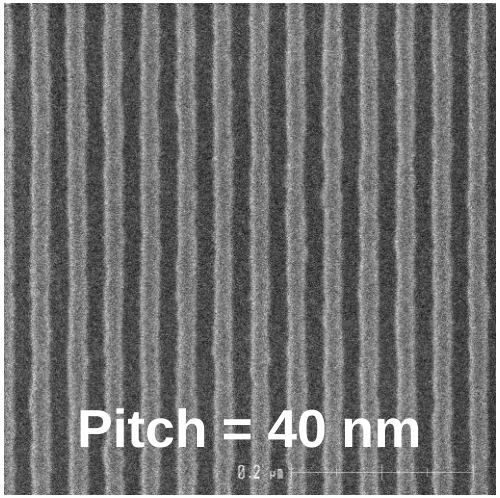


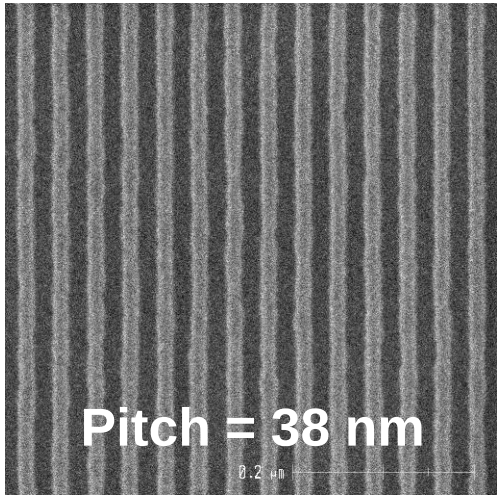
Throughput : 8 wph using ASML's ATP procedure

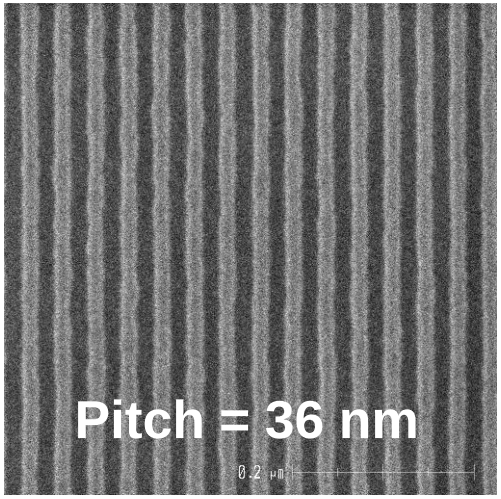
Resolution Limit of NXE3100

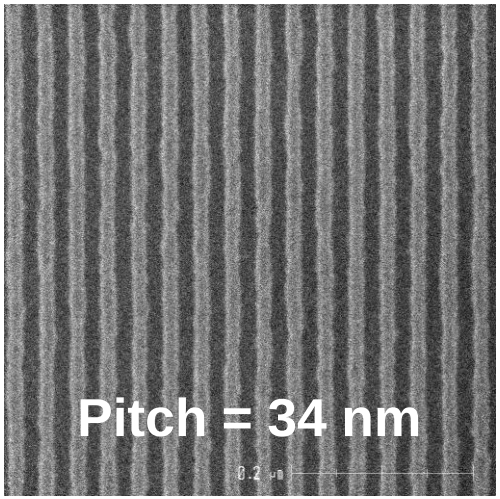
with dipole illumination

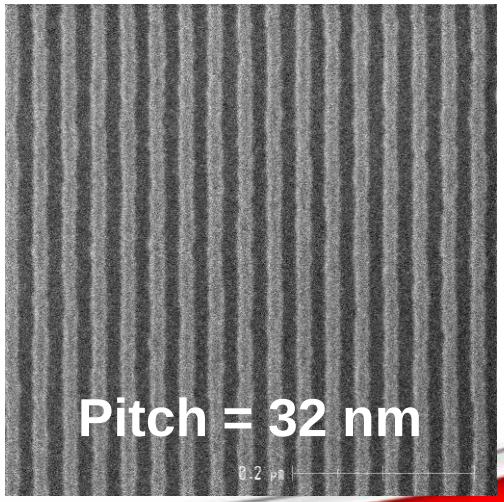




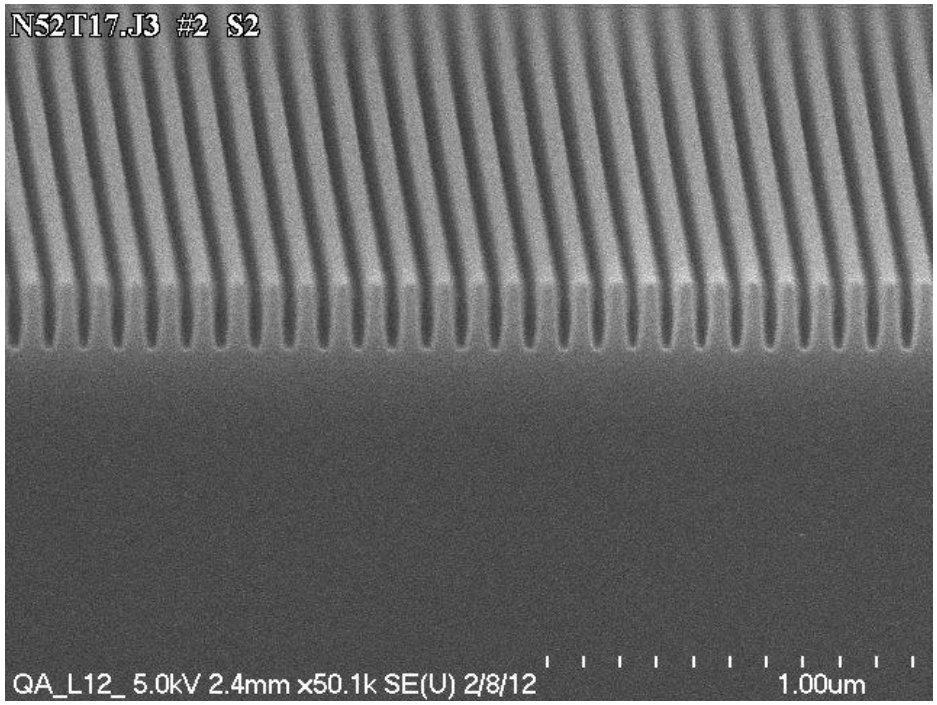


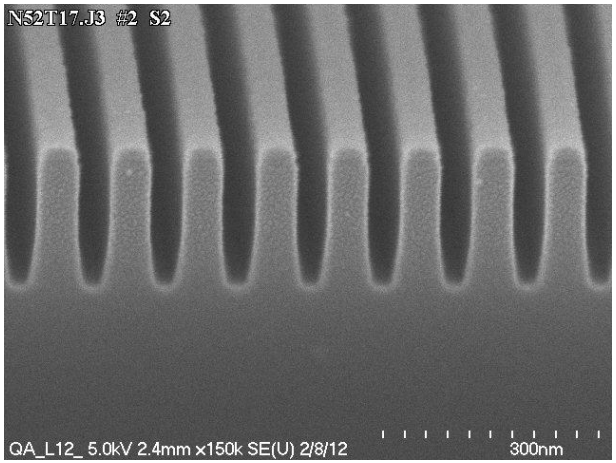






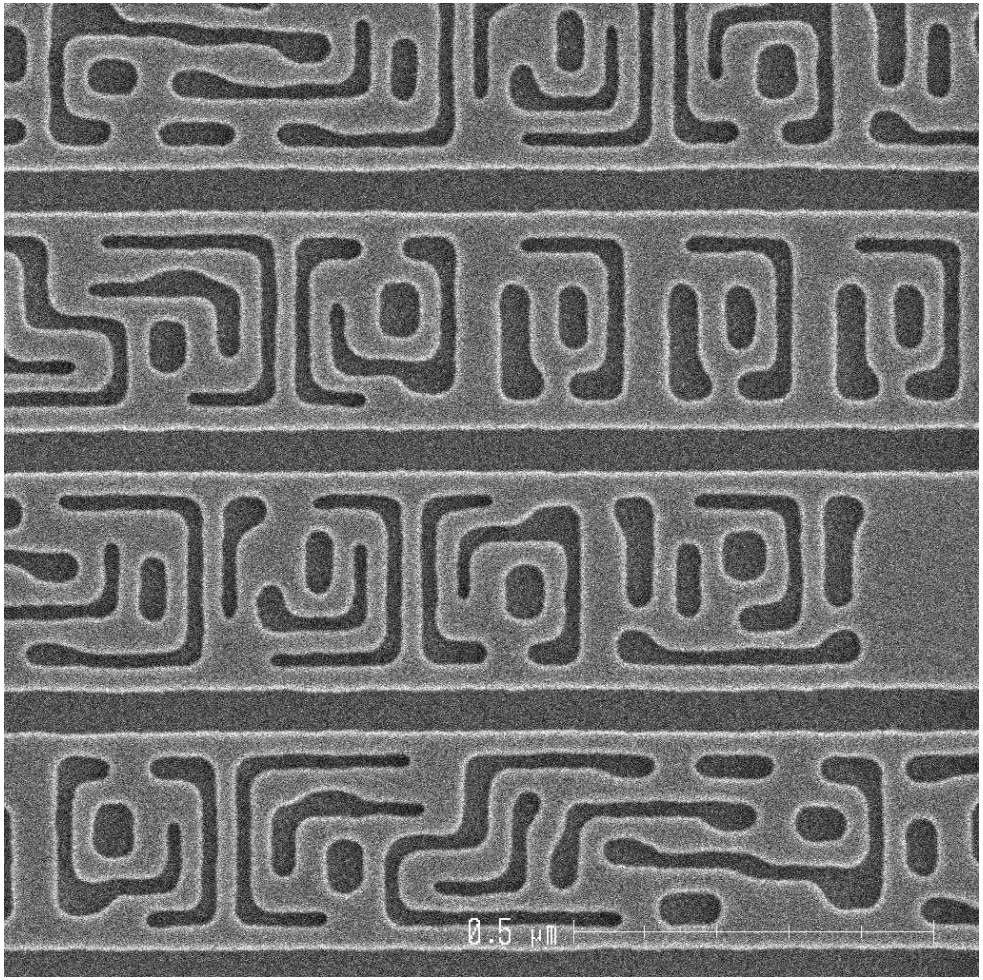
EUV definition of spaces etched into silicon





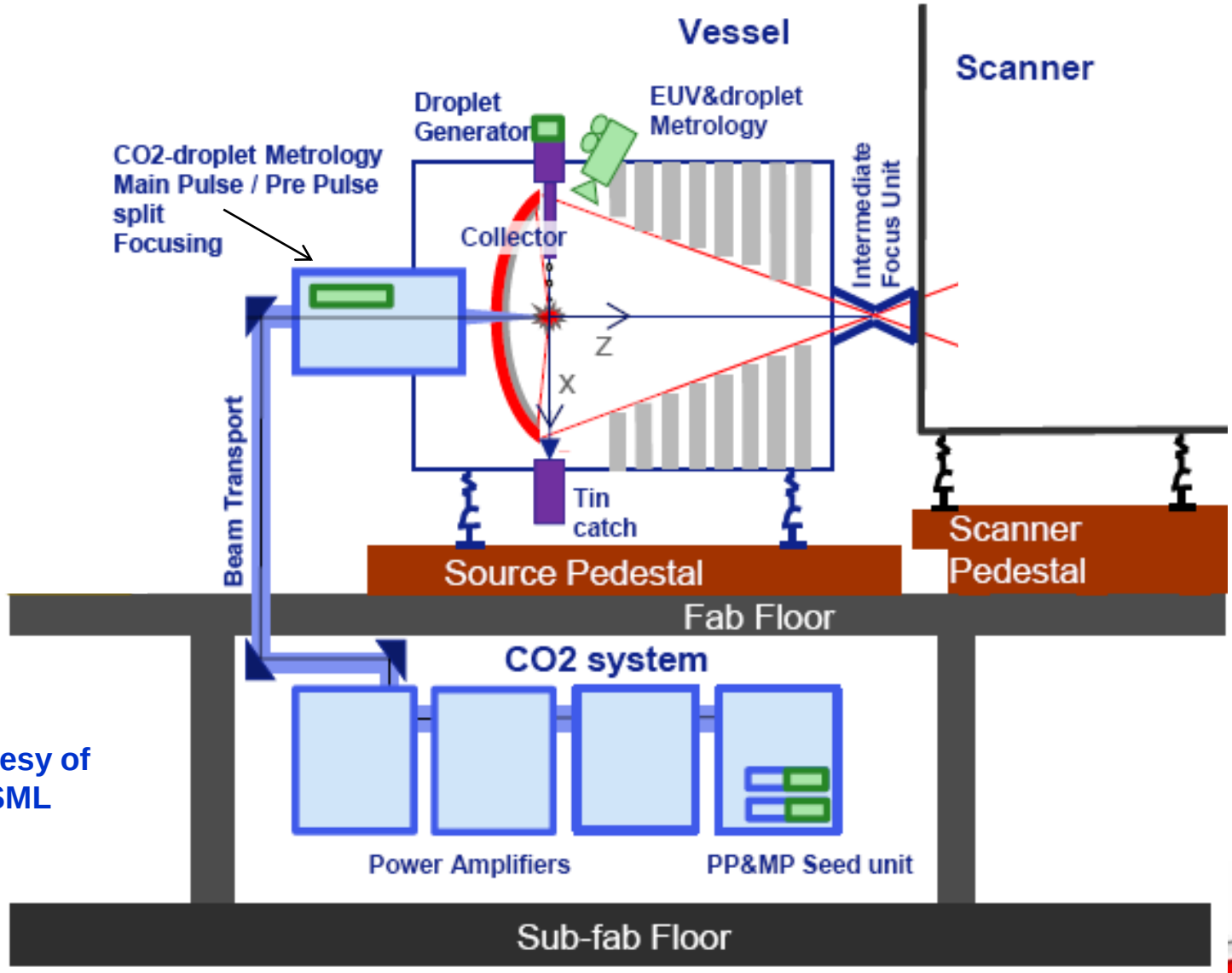
Pitch = 46 nm; NA = 0.25; quadrupole illumination

EUV processing of metal layer of logic circuit



After hard-mask etch-through

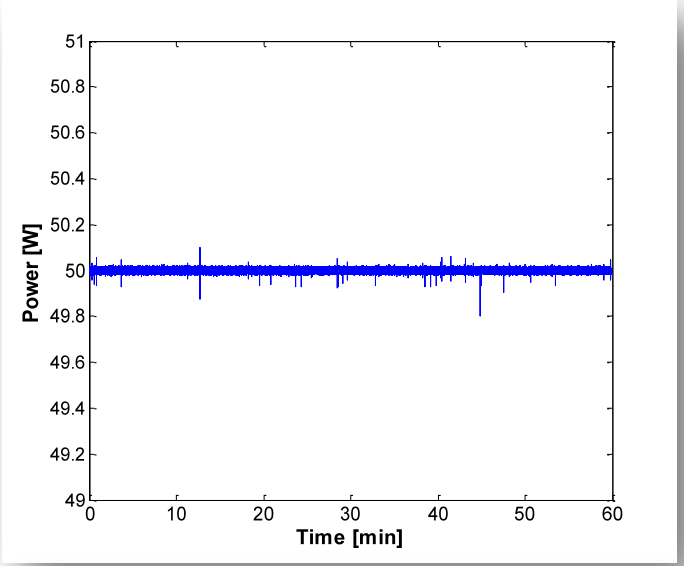
Laser-Produced Plasma EUV Source

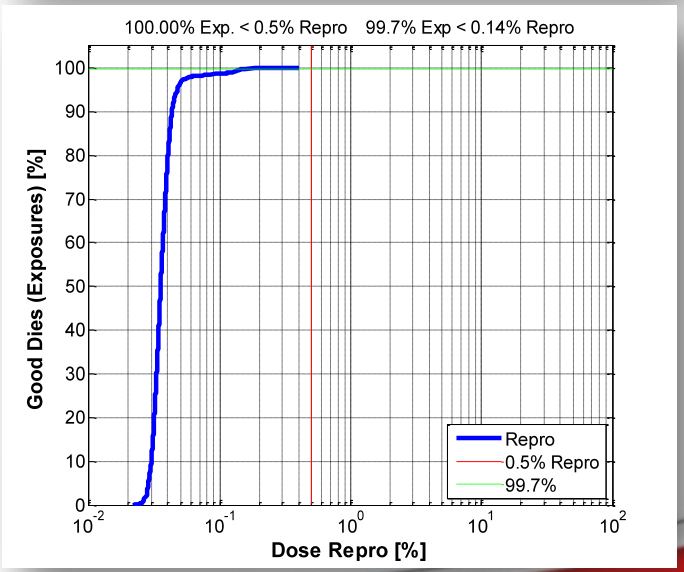


Courtesy of ASML

EUV Source Power

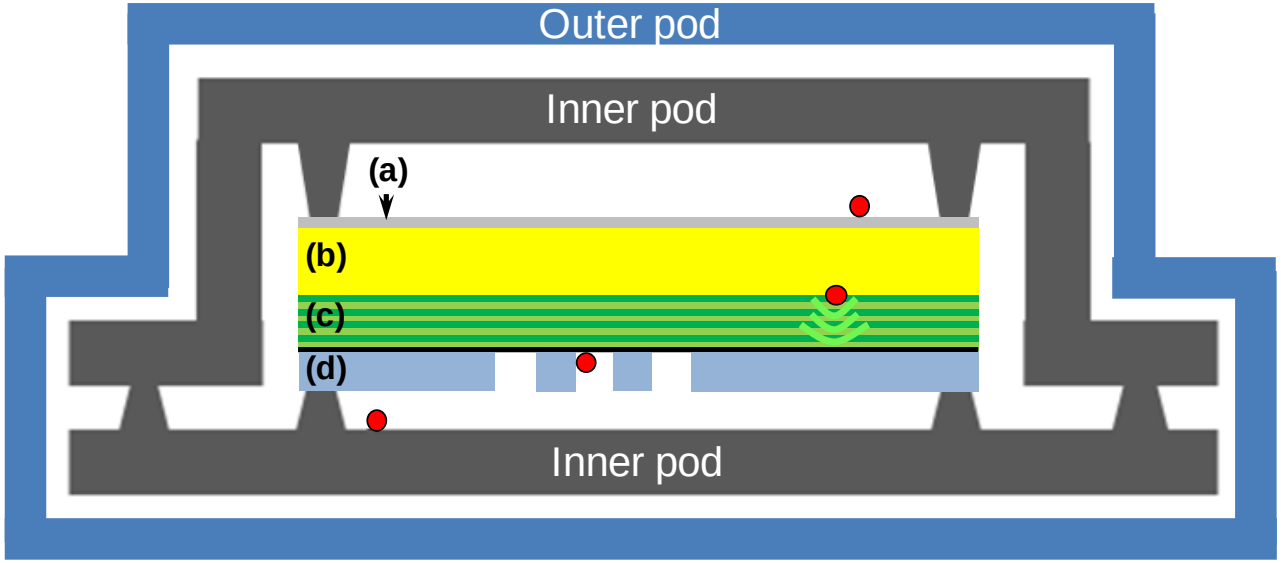
- **Status**
  - 50 W with <±0.5% Dose Stability
  - MOPA + Pre-pulse
  - Dose control in spec over 1 hr. run
    - Die yield exceeded 99.7%
- **Goals**
  - 250 W to yield 125 wph, ATP spec
  - > 250 W for further CoO reduction and increase in exposure energy
    - Time to pay more serious attention to alternative source technologies





Data and Graphs Courtesy of ASML

EUV Mask in a Dual-Pod



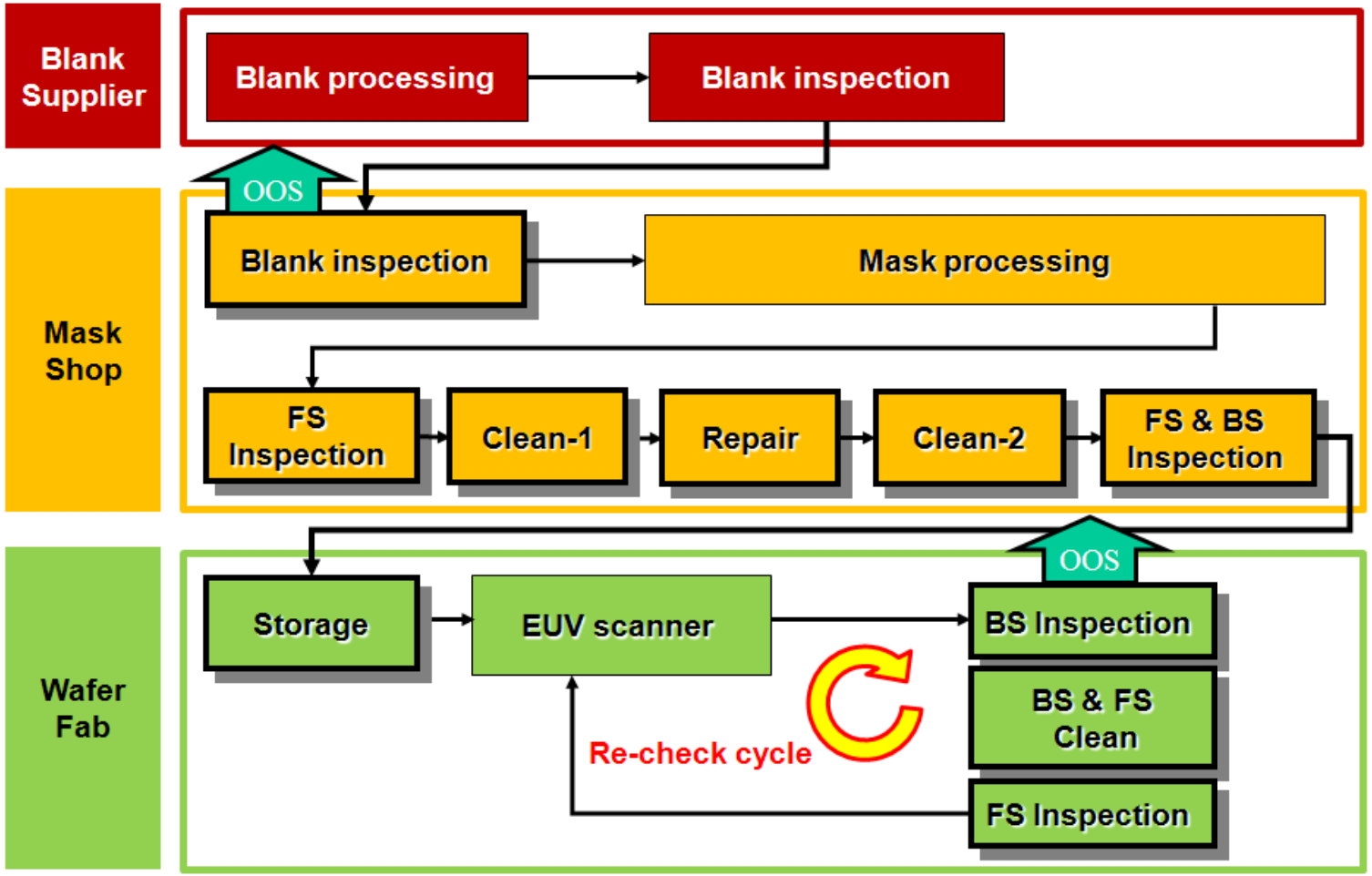
(a) Conductive layer

(b) Low thermal expansion material

(c) Mo/Si multilayer

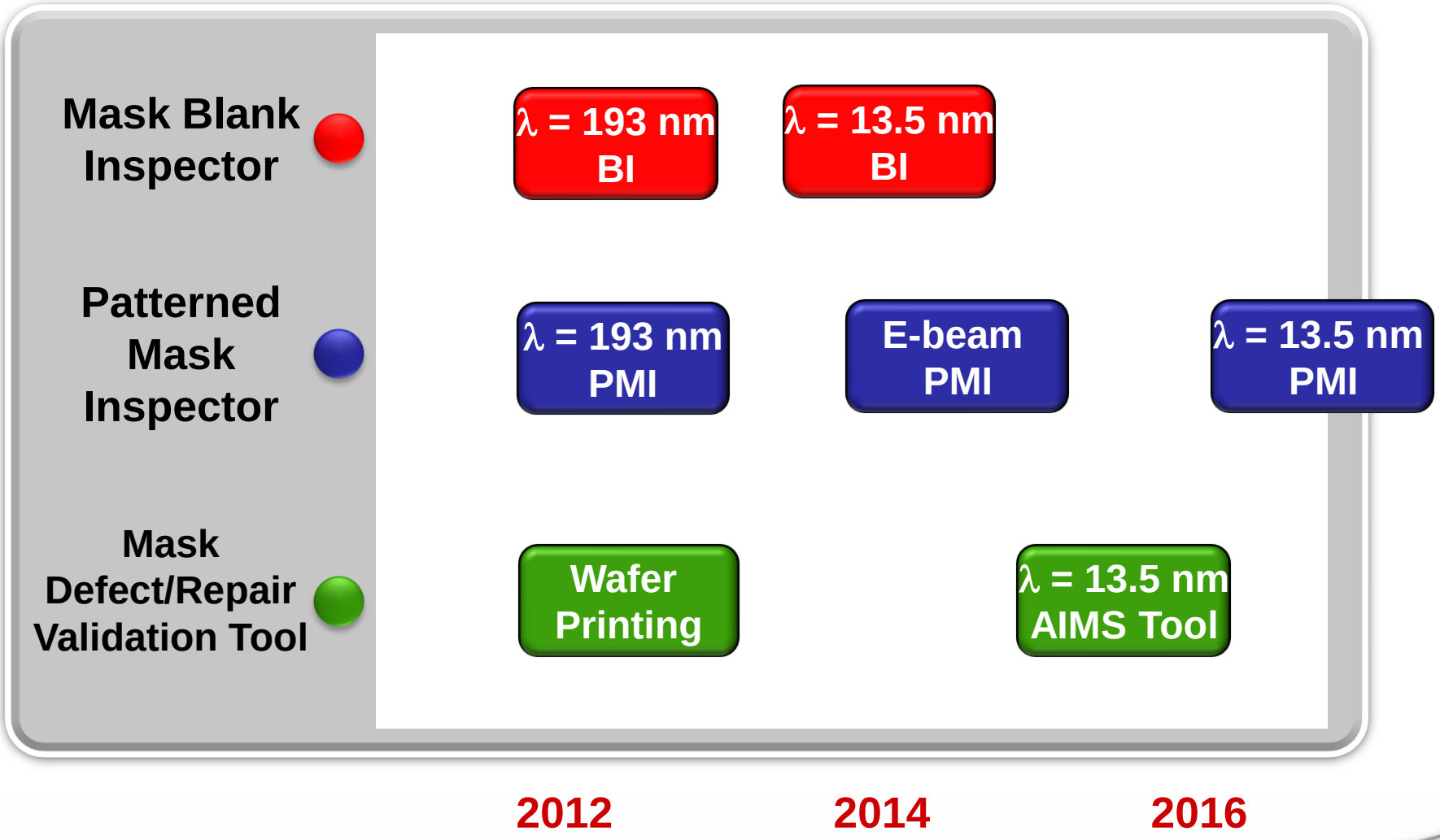
(d) Absorber

Life Cycle of a EUV Mask



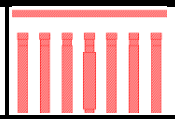
OOS: Out of Spec; FS: Front Side; BS: Back Side

Key equipment in EUV mask metrology

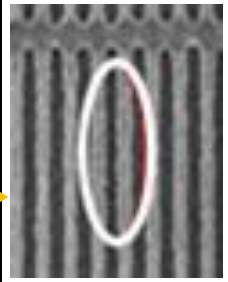


Patterned-EUV-mask Inspection

Detection resolution of a DUV inspector

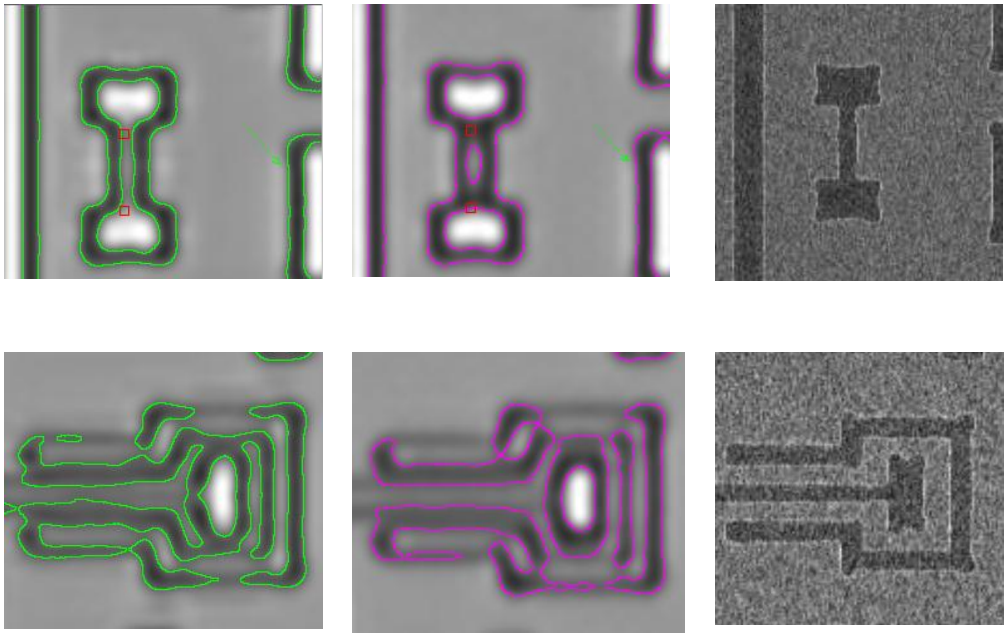
Pattern shift		Programmed defect size on mask (nm)	4	5	6	7	8	9	10	11	12	13	14	15	16	X
		High-sensitivity setting														
		Low-sensitivity setting														
CD-over		Programmed defect size on mask (nm)	6	8	10	12	14	16	18	20	22	24	26	28	30	X
		High-sensitivity setting														
		Low-sensitivity setting														
CD-under		Programmed defect size on mask (nm)	-6	-8	-10	-12	-14	-16	-18	-20	-22	-24	-26	-28	-30	X
		High-sensitivity setting														
		Low-sensitivity setting														
Extursion		Programmed defect size on mask (nm)	56	64	72	80	88	96	104	112	120	128	136	144	152	X
		High-sensitivity setting														
		Low-sensitivity setting														
Pin-hole		Programmed defect size on mask (nm)	28	32	36	40	44	48	52	56	60	64	68	72	76	X
		High-sensitivity setting														
		Low-sensitivity setting														
Intrusion		Programmed defect size on mask (nm)	56	64	72	80	88	96	104	112	120	128	136	144	152	X
		High-sensitivity setting														
		Low-sensitivity setting														
Pin-dot		Programmed defect size on mask (nm)	28	32	36	40	44	48	52	56	60	64	68	72	76	X
		High-sensitivity setting														
		Low-sensitivity setting														

SEM image on wafer



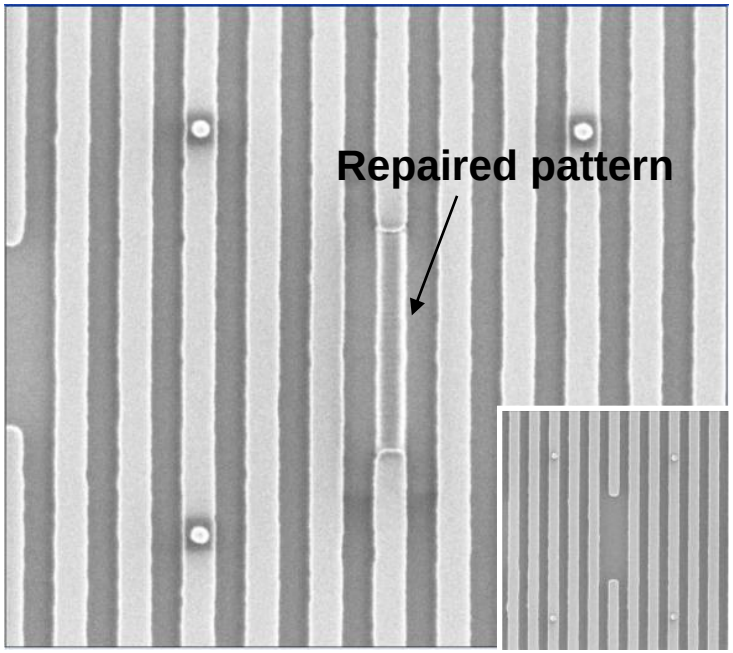
False defects in EUV mask pattern inspection

Rendered images	Inspection images	Mask SEM images

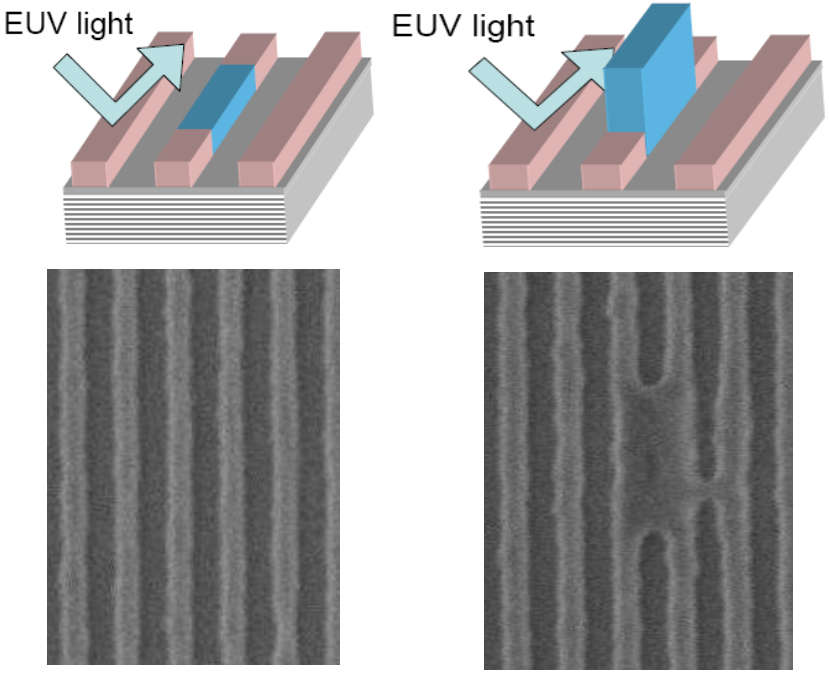


More accurate optical modeling is needed for better image rendering to further minimize false defects

3D profile control is key in EUV mask repair



Mask SEM image



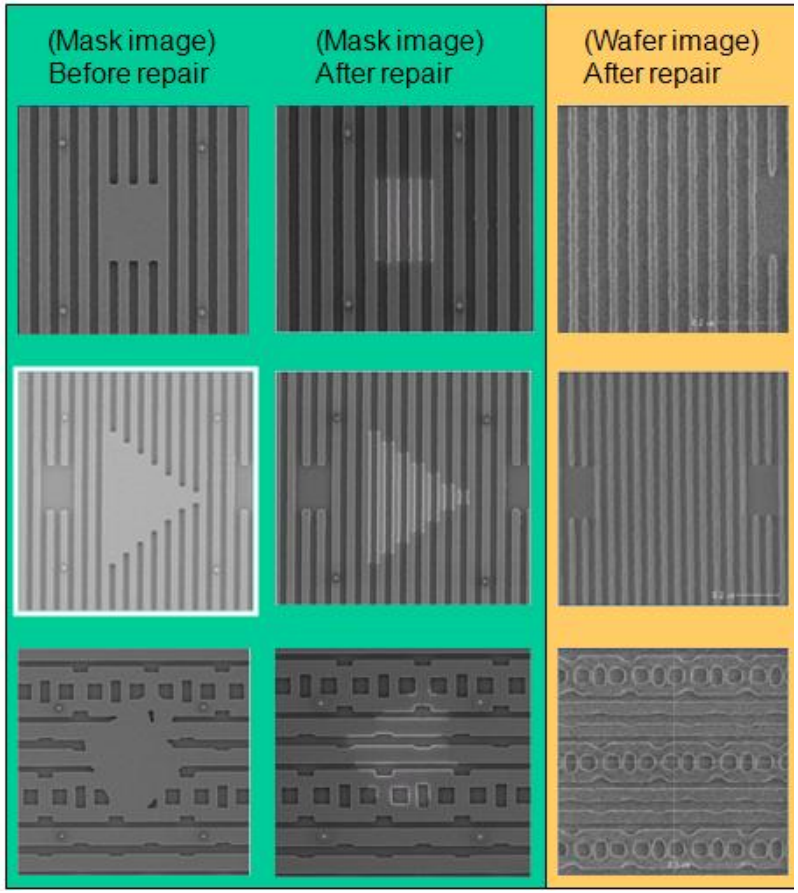
Perfectly repaired

Shadow effect is observed!

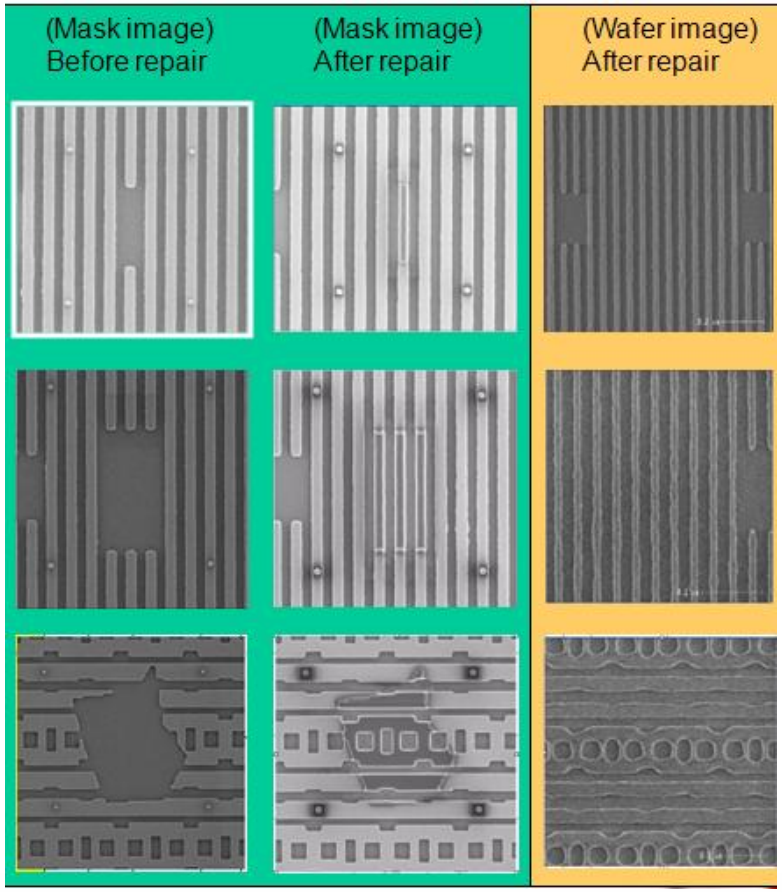
Wafer printing results

EUV absorber defects are repairable

Opaque Defects

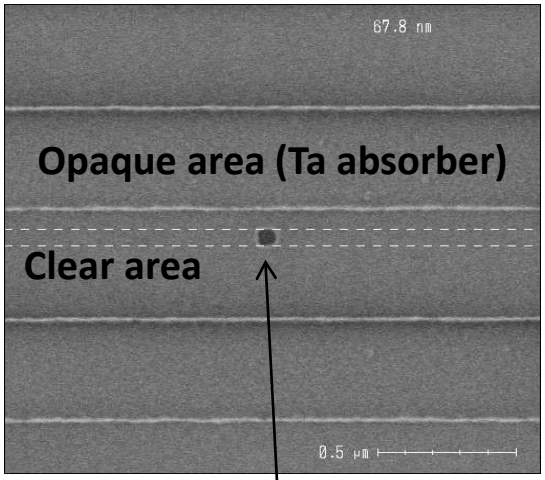


Clear (Missing) Defects



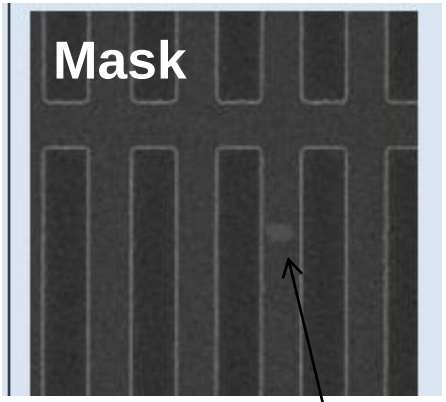
Mitigation of mask blank defects by a global shift of mask patterns

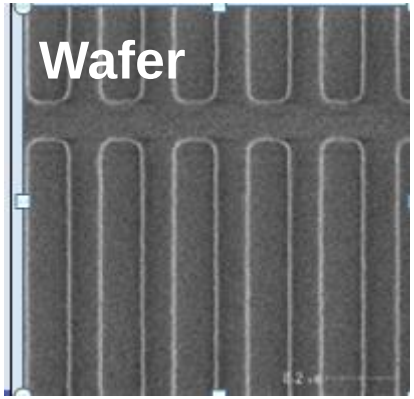
Without pattern shift



This blank defect (~70nm on mask) is in the clear area and will be printed on wafer

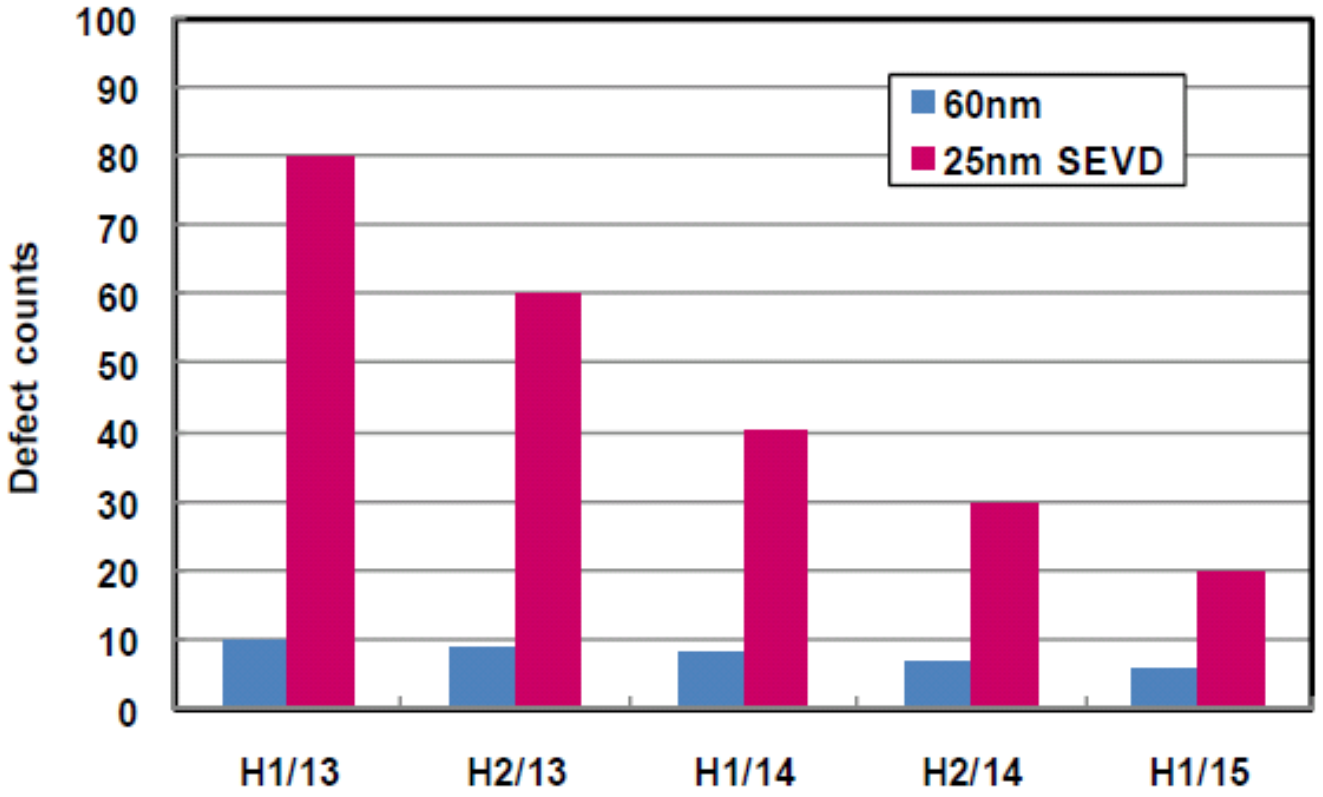
With pattern shift





After global pattern shift, a blank defect shown above is now hidden beneath the Ta absorber

EUV mask blank defect reduction roadmap

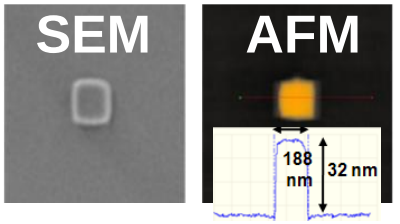


Courtesy of HOYA Corporation

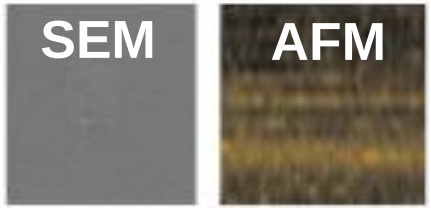
Use of Nano-machining and electron-beam mask repair tools to eliminate bumps and pits on LTEM substrates

Elimination of bump defect on LTEM

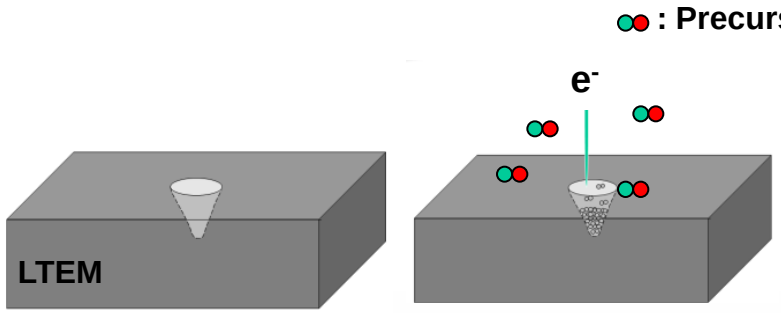
Before



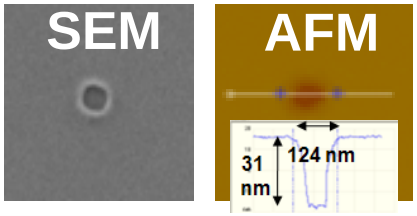
After



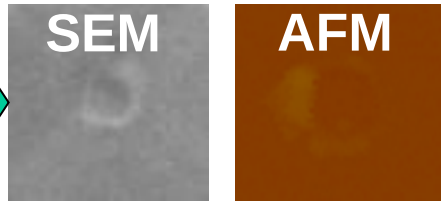
Elimination of pit defect on LTEM



Before

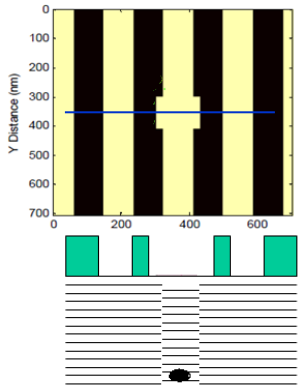


After



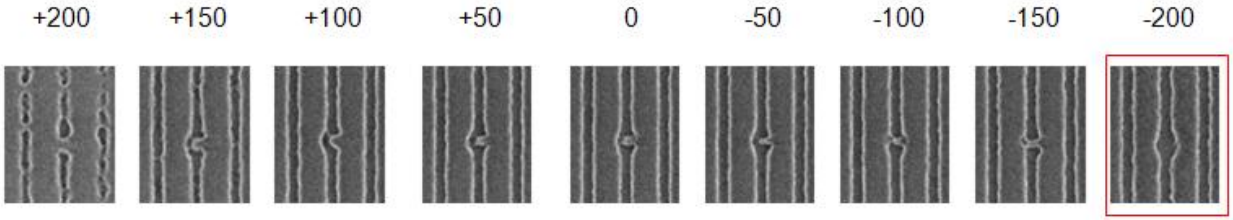
Compensation of mask blank defects

Absorber pattern on mask



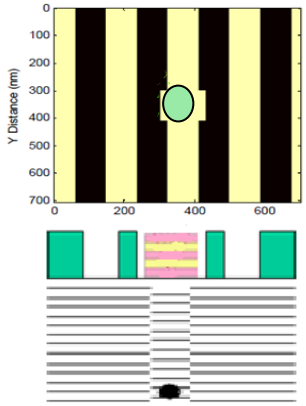
Cross Section

Usual compensation repair: wafer image



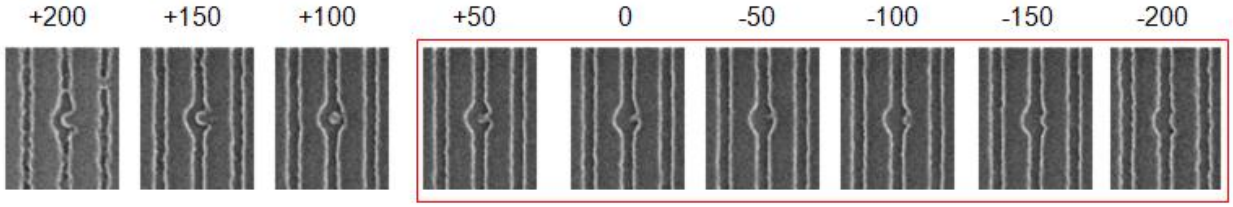
Defocus (nm)

Absorber patterns on mask



Cross section

Novel compensation repair: wafer image

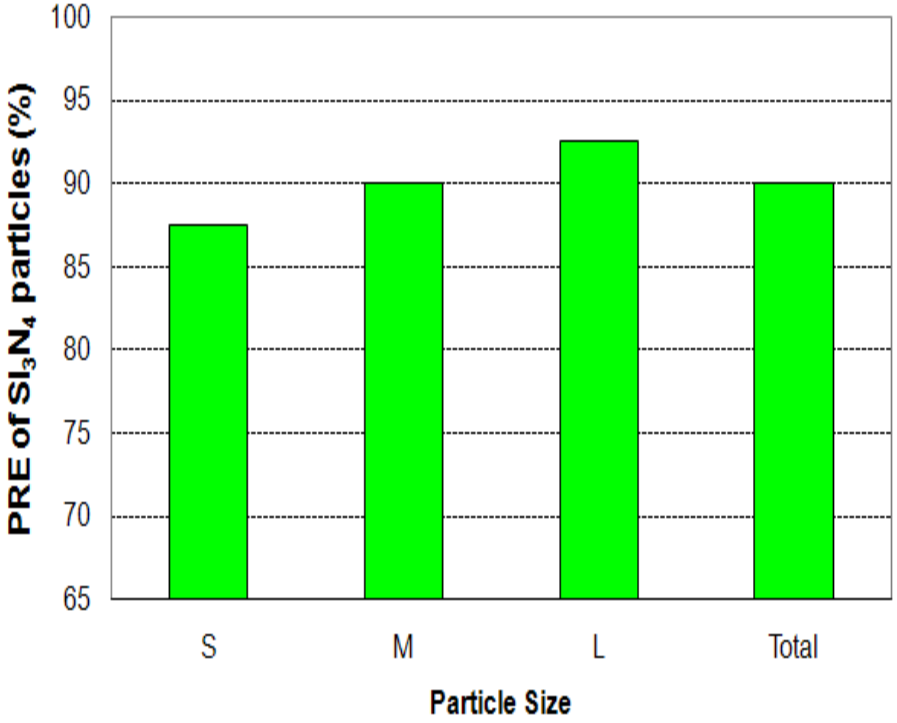


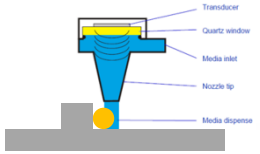
Defocus (nm)

Compensation repair aims to form a more tolerable image on wafer

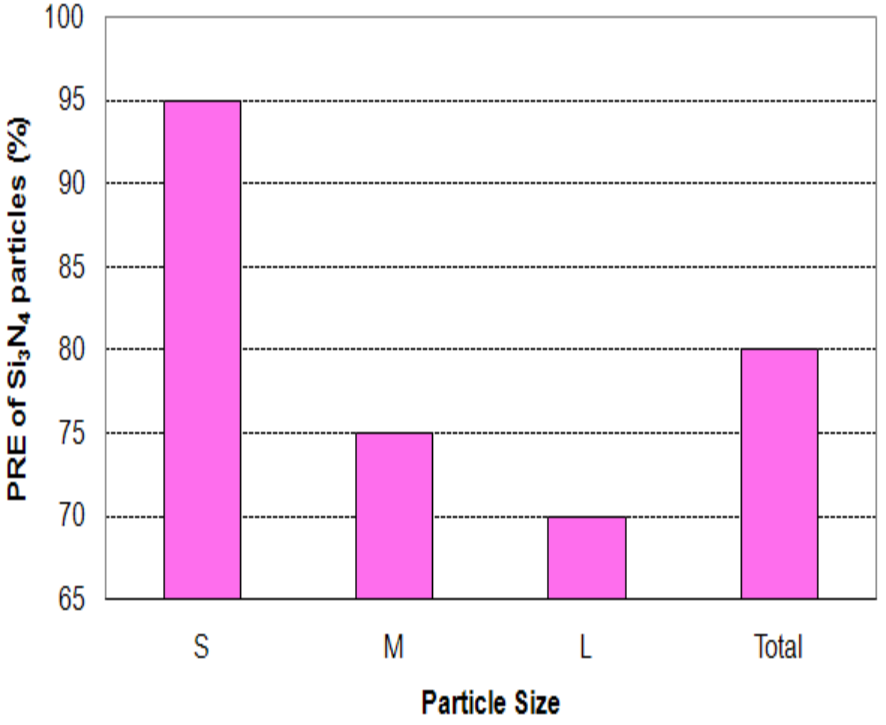
PRE enhancement in mask cleaning using complementary physical force

Spray Cleaning



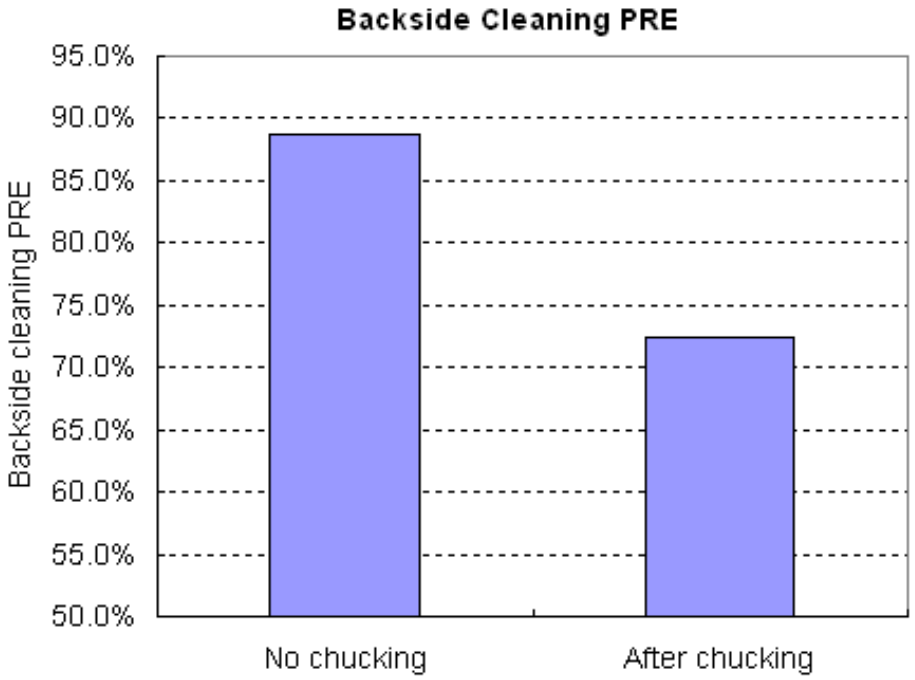


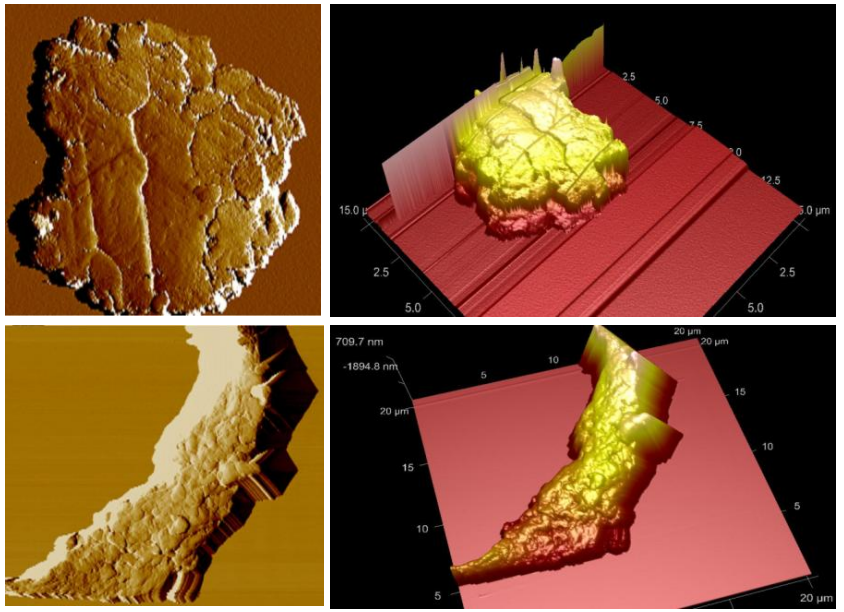
Megasonic Cleaning



Particle size S: 40~80 nm; M: 81~150 nm; L: >150 nm

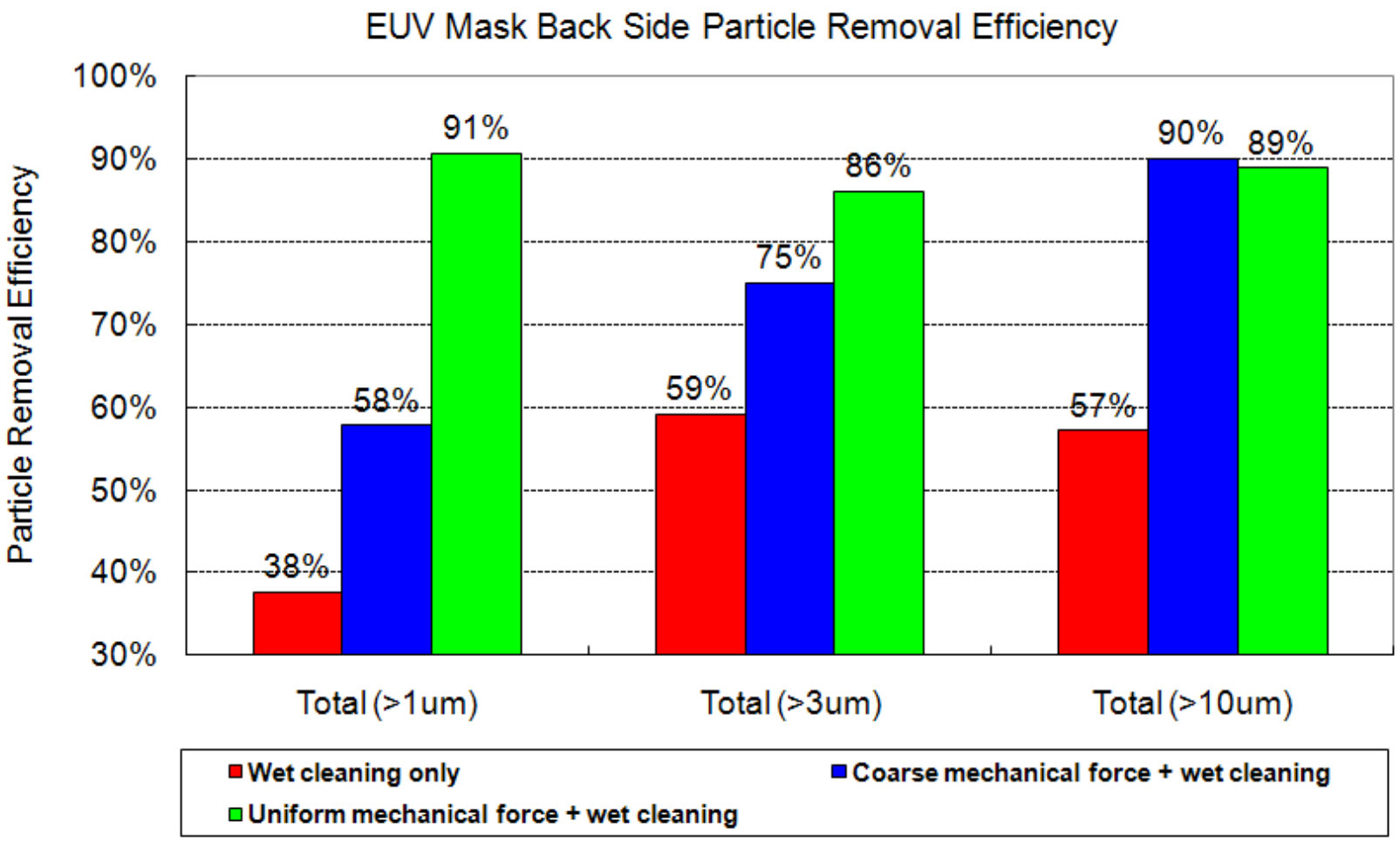
Conventional mask cleaning cannot easily remove compressed particles on the back side





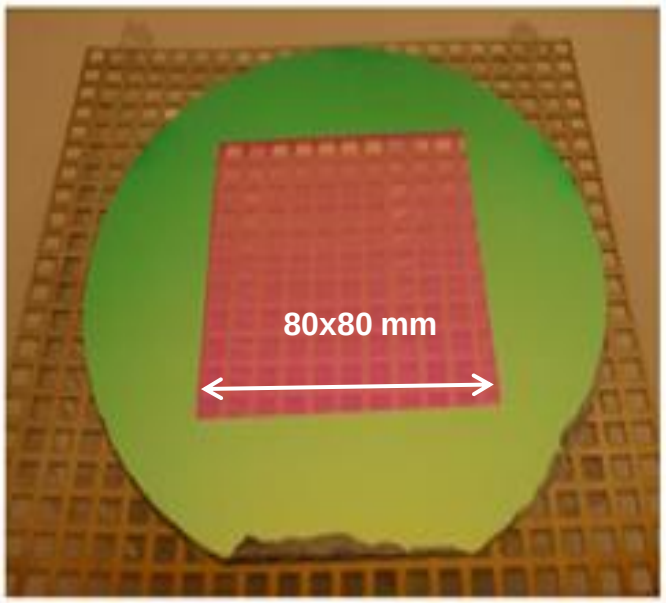
AFM images of post-chucking back-side particles

Mechanical-force cleaning of mask back side



Progress on Pellicles for EUV Masks

- **Requirements**
  - **> 90% EUV transmission**
  - **110 x 144 mm² in size**
- **Progress**
  - **Polysilicon membrane**
    - **55 nm in thickness**
  - **> 82% EUV transmission**
  - **80 x 80 mm² in size**



Data and Photo Courtesy of ASML

- **Remaining Challenges/Opportunities**
  - **Turn membrane into a pellicle**
  - **Commercial suppliers to take over**

To Make EUV HVM a Reality

- Progress towards 250 W source power must not slow down
  - 80-W target by end of 2013 must happen
  - 250-W scanners should be operational in 2015
- Native defects in mask blanks must be further reduced by an order of magnitude
  - From best-case ~100 today to mostly ~10 (at ~30 nm in size)
  - Suppliers must make necessary investments in new and dedicated processing tools for blank fabrication
- Continuous progress must take place on realizing EUV pellicles (110 x 144 mm^2 in size)
  - Must be > 90% per-pass transparency
  - Potential commercial suppliers should seize this opportunity and not withdraw from the challenge